Freerunning represents the first step in troubleshooting a microprocessor-based board using signature analysis (SA). Freerunning essentially involves breaking all feedback paths from the board’s circuits to the microprocessor and forcing the microprocessor to permanently execute a single-byte instruction that causes continuous cycling through the entire address field. The circuitry that implements the freerun mode is often referred to as the *kernel*. Without correct performance of the kernel, further SA troubleshooting proves impossible.

With fully synchronous 8-bit microprocessors, engineers can easily design the freerunning capability into a µP system. And even with µP boards not designed for testability with SA techniques, simple test fixtures can accomplish freerun.

With the advent of 16-bit microprocessors, asynchronous bus control became a common feature. Different peripheral devices and types of memory can interface to the µP asynchronously. However, the read and write cycle times of such devices differ from each other, which must be taken into account when designing the microprocessor freerun fixture.

**The M68000 freerun fixture**

The M68000 µP handles asynchronous data transfers via the following control signals: address strobe (AS), read/write (R/W), upper and lower data strobes (UDS, LDS), and data transfer acknowledge (DTACK). Since the freerun mode forces a constant single-word (16-bit) instruction, R/W will be high, indicating that the microprocessor is reading the instruction operation code (op code). The DTACK signal is activated after the data transfer, either in a read or write cycle. Due to the different read and write cycle times of the memory and peripheral devices on the board, DTACK is activated with different time delays after the microprocessor activates the AS output. Consequently, the freerun fixture must permit generating DTACK with jumper-selectable time delays in order to adjust the read cycle to the speed of the devices on the board under test. The selected time delay should support the read and write cycle of the slowest device on the board.

As shown in the diagram of the M68000 freerun fixture, the 8-bit parallel output serial shift register (74LS164) is used to generate delayed DTACK after the µP activates AS. The jumper can select eight possible time delays, ranging from a ½ clock period to 7½ clock periods.

Due to its even op code (hex 2040), instruction MOVE D0 A0 has been selected to force the freerun. The operation demands an even op-code instruction because during the reset operation, the µP reads the contents on the data bus and treats it as the reset address. An odd op code could cause the microprocessor to detect the word access with an odd address error condition, and the freerun operation could not start.

In signature analysis, the troubleshotter connects the START and STOP probes of a signature analyzer to A23 (pin 52) and then connects the CLOCK probe to AS (pin 6); the signatures read on the address lines appear in the diagram.

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